AMENDMENTS TO THE CLAIMS

Claim Nos. 1, 6, 10, 35, 40, and 44 have been amended. No claims have been canceled, and no claims have been added. A listing of claims follows:

Listing of Claims:

1. (Currently Amended) A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

initializing a first and second subset of a set of per-alignment state machines in a shared memory;

receiving a first and second signal; and

simultaneously sync hunting the first signal with the first subset of the set of per-alignment state machines and the second signal with the second subset of the set of per-alignment state machines.

2. (Original) The machine-readable medium of claim 1 wherein the first and second signal have different formats.

3. (Previously Presented) The machine-readable medium of claim 1 wherein the sync hunting includes updating a first and second set of states indicated by the first and second subset of the set of per-alignment state machines and writing the updated first set of states to the first subset of per-alignment state machines and the updated second set of states to the second subset of per-alignment state machines.

4. (Original) The machine-readable medium of claim 1 further comprising buffering a first set of states from the first subset of the set of per-alignment state machines and a second set of states from the second subset of the set of per-alignment state machines.

5. (Original) The machine-readable medium of claim 1 further comprising:

updating a first and second set of states from the first and second subset of the set of per-alignment state machines;

buffering the first and second set of states; and

writing the first set of states to the first subset of the set of per-alignment state machines; and

writing the second set of states to the second subset of the set of per-alignment state machines.

6. (Currently Amended) A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

initializing a first and second subset of a set of per-alignment state machines in a shared memory;

receiving a first and second signal;

buffering a first and second set of states from the first and second subset of the set of per-alignment state machines;

simultaneously sync hunting the first signal with the first set of states and the second signal with the second set of states.

7. (Original) The machine-readable medium of claim 6 wherein the first and second signal have different formats.

8. (Previously Presented) The machine-readable medium of claim 6 wherein the sync hunting includes updating the first and second set of states and writing the updated first set of states to the first subset of per-alignment state machines and the updated second set of states to the second subset of per-alignment state machines.

9. (Original) The machine-readable medium of claim 6 further comprising:

updating the first and second set of states;

buffering the first and second set of states;

writing the updated first set of states to the first subset of per-alignment state machines; and

writing the updated second set of states to the second subset of per-alignment state machines.

10. (Currently Amended) A machine-readable medium that provides instructions, which when executed by a set of processors, cause said set of processors to perform operations comprising:

initializing a first subset of a set of per-alignment state machines in a shared memory;

receiving a first signal;

initializing a second subset of the set of per-alignment state machines in said shared memory;

receiving a second signal;

buffering a first set of states from the first subset of per-alignment state machines;

buffering a second set of states from the second subset of per-alignment state machines;

simultaneously sync hunting the first signal with the first set of states and the second signal with the second set of states.

11. (Original) The machine-readable medium of claim 10 wherein the first and second signal have different formats.

12. (Previously Presented) The machine-readable medium of claim 10 wherein the sync hunting includes updating the first and second set of states and writing the updated first set of states to the first subset of per-alignment state machines and the updated second set of states to the second subset of per-alignment state machines.

13. (Original) The machine-readable medium of claim 10 further comprising:

updating the first and second set of states;

buffering the first and second set of states;

writing the updated first set of states to the first subset of per-alignment state machines; and

writing the updated second set of states to the second subset of per-alignment state machines.

14. (Previously Presented) An apparatus comprising:

a first sync hunt logic to sync hunt a first signal;

a second sync hunt logic to sync hunt a second signal;

a memory controller coupled with the first and second sync hunt logics, the memory controller to perform read and write operations between the first and second sync hunt logics and a memory unit; and

the memory unit coupled with the memory controller, the memory unit to store a set of per-alignment state machines.

15. (Previously Presented) The apparatus of claim 14 wherein the first and second sync hunt logics are for a first and second signal format, respectively.

16. (Previously Presented) The apparatus of claim 14 wherein the first sync hunt logic includes:

a read buffer coupled to the memory controller, the read buffer to buffer a first set of states written by the memory controller; and

a write buffer coupled to the memory controller, the write buffer to buffer a second set of states output from the first logic.

17. (Previously Presented) The apparatus of claim 14 wherein the second sync hunt logic includes:

a read buffer coupled to the memory controller, the read buffer to buffer a first set of states written by the memory controller; and

a write buffer coupled to the memory controller, the write buffer to buffer a second set of states output from the second logic.

18. (Previously Presented) The apparatus of claim 14 further comprising:

a write buffer coupled to the first and second sync hunt logics and the memory controller, the write buffer to buffer a first set of states written by the memory controller; and

a read buffer coupled to the first and second sync hunt logics and the memory controller, the read buffer to buffer a second set of states, the second set of states written to the read buffer by the first and second logic.

19. (Previously Presented) The apparatus of claim 14 further comprising:

the first sync hunt logic to update a first set of states from the memory unit;

the second sync hunt logic to update a second set of states from the memory unit;

a first buffering unit coupled to the memory controller and the first sync hunt logic, the first buffering unit to buffer the first set of states written from the memory unit by the memory controller and to buffer the updated first set of states from the first sync hunt logic; and

a second buffering unit coupled to the memory controller and the second sync hunt logic, the second buffering unit to buffer the second set of states written from the memory unit by the memory controller and to buffer the updated second set of states from the second sync hunt logic.

20. (Previously Presented) An apparatus comprising:

a memory unit to store a set of per-alignment state machines;

a memory controller coupled with the memory unit, the memory controller to perform read and write operations between the memory unit and a plurality of sync hunt logic; and

the plurality of sync hunt logic coupled with the memory controller, the plurality of sync hunt logic to simultaneously perform sync hunting for a plurality of signals with the set of per-alignment state machines.

21. (Previously Presented) The apparatus of claim 20 wherein the plurality of signals have different formatting.

22. (Previously Presented) The apparatus of claim 20 wherein each of the plurality of sync hunt logic includes:

a read buffer coupled with the memory controller, the read buffer to buffer a first set of states written by the memory controller; and

a write buffer coupled with the memory controller, the write buffer to buffer a second set of states to be written to the memory unit by the memory controller.

23. (Previously Presented) The apparatus of claim 20 further comprising:

a write buffer coupled with the plurality of logic and the memory controller, the write buffer to buffer a first set of states written by the memory controller; and

a read buffer coupled with the plurality of logic and the memory controller, the read buffer to buffer a second set of states, the second set of states written to the read buffer by the plurality of sync hunt logic.

24. (Previously Presented) The apparatus of claim 20 further comprising:

the plurality of sync hunt logic to update a set of states from the memory unit; and

a buffering unit coupled with the memory controller and the plurality of logic, the buffering unit to buffer the set of states written from the memory unit by the memory controller and to buffer the updated set of states from the plurality of sync hunt logic.

25. (Original) An apparatus comprising:

a memory unit to store a set of per-alignment state machines;

a memory controller coupled to the memory unit to access the set of per-alignment state machines;

a first deframing slice coupled to the memory controller, the first deframing slice to sync hunt a first signal with a first subset of the set of per-alignment state machines; and

a second deframing slice coupled to the memory controller, the second deframing slice to sync hunt a second signal with a second subset of the set of per-alignment state machines.

26. (Original) The apparatus of claim 25 wherein the first and second signal have different signal formatting.

27. (Previously Presented) The apparatus of claim 25 wherein the first deframing slice includes a first sync hunt logic for a first signal format and a second sync hunt logic for a second signal format.

28. (Original) The apparatus of claim 25 wherein the first deframing slice includes:

a read buffer coupled to the memory controller, the read buffer to buffer a first set of states from the first subset of per-alignment state machines written by the memory controller; and

a write buffer coupled to the memory controller, the write buffer to buffer a second set of states output from the first deframing slice.

29. (Original) The apparatus of claim 25 wherein the second deframing slice includes:

a read buffer coupled to the memory controller, the read buffer to buffer a first set of states from the second subset of per-alignment state machines written by the memory controller; and

a write buffer coupled to the memory controller, the write buffer to buffer a second set of states output from the second deframing slice.

30. (Original) The apparatus of claim 25 further comprising:

a write buffer coupled to the first and second deframing slice and the memory controller, the write buffer to buffer a first set of states written by the memory controller; and

a read buffer coupled to the first and second deframing slice and the memory controller, the read buffer to buffer a second set of states, the second set of states written to the read buffer by the first and second deframing slice.

31. (Original) The apparatus of claim 25 further comprising:

the first deframing slice to update a first set of states from the memory unit;

the second deframing slice to update a second set of states from the memory unit;

a first buffering unit coupled to the memory controller and the first deframing slice, the first buffering unit to buffer the first set of states written from the memory unit by the memory controller and to buffer the updated first set of states from the first deframing slice; and

a second buffering unit coupled to the memory controller and the second deframing slice, the second buffering unit to buffer the second set of states written from the memory unit by the memory controller and to buffer the updated second set of states from the second deframing slice.

32. (Original) An apparatus comprising:

a memory unit to store a set of per-alignment state machines;

a memory controller coupled to the memory unit, the memory controller to access the set of per-alignment state machines;

a first deframing slice coupled to the memory controller, the first deframing slice having

a first set of buffers coupled to the memory controller, the first set of buffers to store a first set of states from a first subset of the set of per-alignment state machines,

a first set of logic coupled to the first set of buffers, the first set of logic to sync hunt a first signal with the first set of states and to update the first set of states,

a second set of buffers coupled to the first set of logic, the second set of buffers to store the updated first set of states, the updated first set of states to be written to the first subset of the set of per-alignment state machines; and

a second deframing slice coupled to the memory controller, the second deframing slice having

a third set of buffers coupled to the memory controller, the third set of buffers to store a second set of states from a second subset of the set of per-alignment state machines,

a second set of logic coupled to the third set of buffers, the second set of logic to sync hunt a second signal with the second set of states and to update the second set of states,

a fourth set of buffers coupled to the second set of logic, the fourth set of buffers to store the updated second set of states, the updated second set of states to be written to the second subset of the set of per-alignment state machines.

33. (Original) The apparatus of claim 32 wherein the first and second signal have different signal formatting.

34. (Original) The apparatus of claim 32 wherein the first deframing slice further comprises a third set of logic for a second signal format, the first set of logic being for a first signal format.

35. (Currently Amended) A computer implemented method comprising:

initializing a first and second subset of a set of per-alignment state machines in a shared memory;

receiving a first and second signal; and

simultaneously sync hunting the first signal with the first subset of the set of per-alignment state machines and the second signal with the second subset of the set of per-alignment state machines.

36. (Original) The computer implemented method of claim 35 wherein the first and second signal have different formats.

37. (Previously Presented) The computer implemented method of claim 35 wherein the sync hunting includes updating a first and second set of states indicated by the first and second subset of the set of per-alignment state machines and writing the updated first set of states to the first subset of per-alignment state machines and the updated second set of states to the second subset of per-alignment state machines.

38. (Original) The computer implemented method of claim 35 further comprising buffering a first set of states from the first subset of the set of per-alignment state machines and a second set of states from the second subset of the set of per-alignment state machines.

39. (Original) The computer implemented method of claim 35 further comprising:

updating a first and second set of states from the first and second subset of the set of per-alignment state machines;

buffering the first and second set of states; and

writing the first set of states to the first subset of the set of per-alignment state machines; and

writing the second set of states to the second subset of the set of per-alignment state machines.

40. (Currently Amended) A computer implemented method comprising:

initializing a first and second subset of a set of per-alignment state machines in a shared memory;

receiving a first and second signal;

buffering a first and second set of states from the first and second subset of the set of per-alignment state machines;

simultaneously sync hunting the first signal with the first set of states and the second signal with the second set of states.

41. (Original) The computer implemented method of claim 40 wherein the first and second signal have different formats.

42. (Previously Presented) The computer implemented method of claim 40 wherein the sync hunting includes updating the first and second set of states and writing the updated first set of states to the first subset of per-alignment state machines and the updated second set of states to the second subset of per-alignment state machines.

43. (Original) The computer implemented method of claim 40 further comprising:

updating the first and second set of states;

buffering the first and second set of states;

writing the updated first set of states to the first subset of per-alignment state machines; and

writing the updated second set of states to the second subset of per-alignment state machines.

44. (Original) A computer implemented method comprising:

initializing a first subset of a set of per-alignment state machines;

receiving a first signal;

initializing a second subset of the set of per-alignment state machines;

receiving a second signal;

buffering a first set of states from the first subset of per-alignment state machines;

buffering a second set of states from the second subset of per-alignment state machines;

simultaneously sync hunting the first signal with the first set of states and the second signal with the second set of states.

45. (Original) The computer implemented method of claim 44 wherein the first and second signal have different formats.

46. (Previously Presented) The computer implemented method of claim 44 wherein the sync hunting includes updating the first and second set of states and writing the updated first set of states to the first subset of per-alignment state machines and the updated second set of states to the second subset of per-alignment state machines.

47. (Original) The computer implemented method of claim 44 further comprising:

updating the first and second set of states;

buffering the first and second set of states;

writing the updated first set of states to the first subset of per-alignment state machines; and

writing the updated second set of states to the second subset of per-alignment state machines.

48. (Previously Presented) A network device comprising:

a first deframing slice having a first high bit rate signal format synchronization hunting logic and a first low bit rate signal format synchronization hunting logic;

a second deframing slice having a second high bit rate signal format synchronization hunting logic and a second low bit rate signal format synchronization hunting logic;

a memory to host a plurality of state machines;

a memory controller coupled with the first and second deframing slices and the memory, the memory controller to perform read and write operations between the low bit rate signal format synchronization hunting logics and the memory; and

a set of one or more machine readable media coupled with the first and second deframing slices, the set of machine readable media having stored therein a set of instructions to cause the first low bit signal format synchronization hunting logic and the second low bit rate signal format synchronization hunting logic to simultaneously synchronization hunt low bit rate signals extracted from different high bit rate signals using the state machines stored in the memory.

49. (Previously Presented) The network device of claim 48 wherein the low bit rate signal format is DS-1.

50. (Previously Presented) The network device of claim 48 wherein the state machines are per-alignment state machines.